REMARKS

Rejections Under 35 U.S.C. § 112

Claims 1-2 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. In particular, the Examiner stated that "it is not clear which elements of Figure 1A correspond to which limitations of the claims. At present, the connectivity shown in Figure 1A and described on page 6 of the specification does not appear to be the same as what is claimed."

Applicant respectfully traverses the rejection. Applicant maintains that claims 1-2 contain subject matter that was described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. The Applicant further submits that, at least, Figure 32, illustrating a block diagram of a system according to one embodiment of the invention and the Application at page 46, lines 25-28, detail the limitations recited in claims 1-2. The Applicant notes that Figure 1A details a block diagram of a synchronous flash memory embodiment of the present invention and that claims 1-2 are directed to a computer system.

The Applicant respectfully submits that it is analysis of the claim rejected against the Application as a whole that determines enablement under 35 U.S.C. § 112, first paragraph. *See,* MPEP §2163(II)(A)(2) and MPEP §2163(II)(A)(3)(a).

Furthermore, "[w]hat is conventional or well known to one of ordinary skill in the art need not be disclosed in detail. See *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d at 1384, 231 USPQ at 94. If a skilled artisan would have understood the inventor to be in possession of the claimed invention at the time of filing, even if every nuance of the claims is not explicitly described in the specification, then the adequate description requirement is met. See, e.g., *Vas-Cath*, 935 F.2d at 1563, 19 USPQ2d at 1116; *Martin v. Johnson*, 454 F.2d 746, 751, 172 USPQ 391, 395 (CCPA 1972) (stating "the description need not be *in ipsis verbis* [i.e., "in the same words"] to be sufficient"). *See,* MPEP §2163(II)(A)(3)(a).

In particular, claim 1 recites a memory controller, a main memory bus, and a synchronous non-volatile memory, which are detailed in the Application, at least, by elements 340, 330, and 320 in Figure 32 and by the Specification at page 46, lines 25-28.

Claim 2 depends from claim 1, and recites a synchronous non-volatile memory with command interface having a write enable connection (WE#) to receive a write enable signal, a column address strobe connection (CAS#) to receive a column address strobe signal, a row address strobe connection (RAS#) to receive a row address strobe signal, and a chip select connection (CS#) to receive a chip select signal. The limitations of claim 2 are detailed in the Application in, at least, Figures 1A-1C, 4, 6, and 11, and in the Specification at page 3, lines 15-20, page 7, line29 to page 8, line 2, page 20, lines 7-10 and 27-28, page 22, lines 15-20, page 47, lines 9-14, and truth tables 1, 4, and 5.

Rejections Under 35 U.S.C. § 102

Claims 1-2 were rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Bacon et al. (U.S. Patent 5,440,632).

Applicant respectfully traverses this rejection and feels that claims 1-2 are allowable for the following reasons.

Applicant respectfully maintains that Bacon et al. teaches a Flash memory for a reprogrammable subscriber service having a control microprocessor 128, a memory bus 141, and an asynchronous Flash EPROM 134 coupled to the memory bus 141. The Applicant notes that it is well known by those skilled in the art that conventional memory systems are generally divided into asynchronous and synchronous communications. In asynchronous communications the memory controller uses control signals to indicate to the memory when requests for data transactions are sent. The data transfers themselves are also performed asynchronously. These asynchronous communication interactions have difficulty meeting high memory bandwidth demands of many modern computer systems. As a result, synchronous interface standards where the control signals and data transfers are sent at predetermined time periods and in synchronization with a clock

signal have been developed. Examples of these synchronous interfaces include, but are not limited to, Synchronous DRAM (SDRAM) and double data rate SDRAM (DDR-SDRAM). Applicant maintains therefore that because Bacon et al. purports to teach an asynchronous Flash EEPROM, it does not teach or disclose a computer system comprising a memory controller, a main memory bus coupled to the memory controller, and a synchronous non-volatile memory device coupled to the main memory bus. *See, e.g.,* Bacon et al., Figures 2 and 5, and column 8, line 30-39, and column 12, lines 9-34.

Applicant respectfully contends that claim 1 has been shown to be patentably distinct from the cited reference. As claim 2 depends from and further defines claim, it is also considered to be in condition for allowance. Accordingly, Applicant respectfully requests allowance of claims 1-2.

New Claims

Claims 27-38 were added in the present application. Claims 27-33 depend from and further define claim 1. The Applicant submits that therefore claims 27-33 are not anticipated by any of the references made of record and are also considered to be in condition for allowance.

Claim 34 is directed to a computer system comprising a memory controller, a main memory bus coupled to the memory controller, and a synchronous non-volatile memory device coupled to the main memory bus, the synchronous non-volatile memory having a command interface. The command interface having a write enable connection (WE#) to receive a write enable signal, a column address strobe connection (CAS#) to receive a column address strobe signal, a row address strobe connection (RAS#) to receive a row address strobe signal; and a chip select connection (CS#) to receive a chip select signal. The Applicant submits that the elements of claim 34 are not anticipated by any of the references made of record. Therefore the Applicant submits that claim 34 to be in condition for allowance and to contain no new matter. As claims 35-38 depend from and further define claim 34 they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests the consideration and allowance of the new claims 27-38.

CONCLUSION

In view of the above remarks, Applicant respectfully submits that the claims are in condition for allowance and requests reconsideration of the application and allowance of the claims. No new matter has been added and no additional fee is required by this amendment and response.

The Examiner is invited to contact Applicant's representative at the number below if there are any questions regarding this response or if prosecution of this application may be assisted thereby.

Respectfully submitted,

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